



DISTINGUISHED SPEAKER SERIES

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3:35-4:35 pm

22 Deike Building

“Future high-speed and low-power Nanoelectronics”

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ABSTRACT

This presentation will cover three topics. First, it will highlight some of the most recent silicon device and process innovations for enabling and continuing Moore’s Law. Second, it will summarize the research progress on non-silicon transistor channel materials and their integration on silicon substrate for future high-speed and low-power logic CMOS applications.



Third, it will describe the recent research effort on forward-looking devices beyond CMOS. In this beyond-CMOS research space, new devices are being explored to either replace CMOS after 2020 as an alternative switch or combine with CMOS to create new circuit functionalities.

Bio: Robert Chau is an Intel Senior Fellow and director of transistor research and nanotechnology in Intel's Technology and Manufacturing Group. Chau is responsible for directing research and development in advanced transistors and gate dielectrics, process modules and technologies, and silicon integrated processes for microprocessor applications. He is also responsible for leading research efforts in emerging nanotechnology for future nanoelectronics applications. Chau received his bachelor's and master's degrees and Ph.D. in electrical engineering from The Ohio State University. He holds more than 180 issued U.S. patents and has been elected an IEEE Fellow